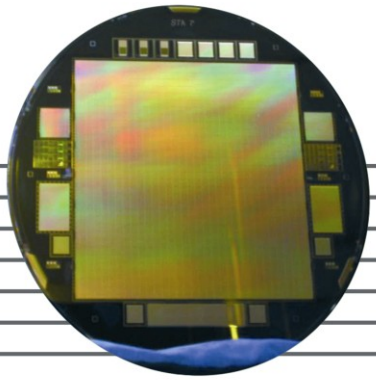


CCD1600A Full Frame CCD Image Sensor 10560 x 10560 Element Image Area

General Description

The CCD1600 is a 10560 x 10560 image element solid state Charge Coupled Device (CCD) Full Frame sensor.

This CCD is intended for use in high-resolution scientific, space based, industrial, and commercial electro-optical systems.

The CCD1600 is organized in two halves each containing an array of 10560 horizontal by 5280 vertical photosites. The pixel spacing is 9µm x 9µm. For dark reference, each readout line is proceeded by 8 dark pixels.

This imager is available in a full frame transfer configuration (shown) or a split frame transfer configuration with shield metalization covering half of the imager. The split frame transfer architecture allows higher frame rate operation through four readout quadrants, whereas the single-sided approach allows readout through two readout quadrants.

The CCD1600 is offered as a backside illuminated version for increased sensitivity and UV response in the same package configuration.

Features

- 10560 x 10560 Photosite Full Frame CCD Array
- 9 µm x 9 µm Pixel
- 95.04mm x 95.04mm Image Area
- 100% Fill Factor
- Readout Noise Less Than 20 Electrons at 10MHz
- Dynamic Range > 75dB
- 16 Two Stage Source Follower Output Channels
- Three-Phase Buried Channel NMOS Image area
- Three-Phase Buried Channel Readout Registers
- Multi-Pinned Phase (MPP) optional

Functional Description

The following functional elements are illustrated in the block diagram:

Image Sensing Elements: Incident photons pass through a transparent polycrystalline silicon gate structure creating electron hole pairs. The resulting photoelectrons are collected in the photosites during the integration period. The amount of charge accumulated in each photosite is a linear function of the localized incident illumination intensity and integration period.

The photosite structure is made up of contiguous CCD elements with no voids or inactive areas. In addition to sensing light, these elements are used to shift image data vertically. Consequently, the device needs to be shuttered during readout.

Vertical Charge Shifting: The Full Frame architecture of the CCD1600 provides video information as a single sequential readout of 5280 lines containing 1320 photosites. At the end of an integration period the ϕA_1, ϕA_2, and ϕA_3 clocks are used to transfer charge vertically through the CCD array to the horizontal readout register. Vertical columns are separated by a channel stop region to prevent charge migration.

The imaging area is divided into an Upper and Lower half. Each 10560 x 5280 halve may be clocked independently or together. Horizontal Transport registers along the top and bottom permit simultaneous readout of both halves. The CCD1600 may be clocked such that the full array is readout by the Upper or Lower Transport registers.

Horizontal Charge Shifting: ϕS_1, ϕS_2 and ϕS_3 are polysilicon gates used to transfer charge horizontally to the output amplifier. The horizontal transport register is twice the size of the photosite to allow for vertical binning. For both frame transfer configurations, the charge may be read out through the eight amplifiers at the bottom or top of the image frame storage region.

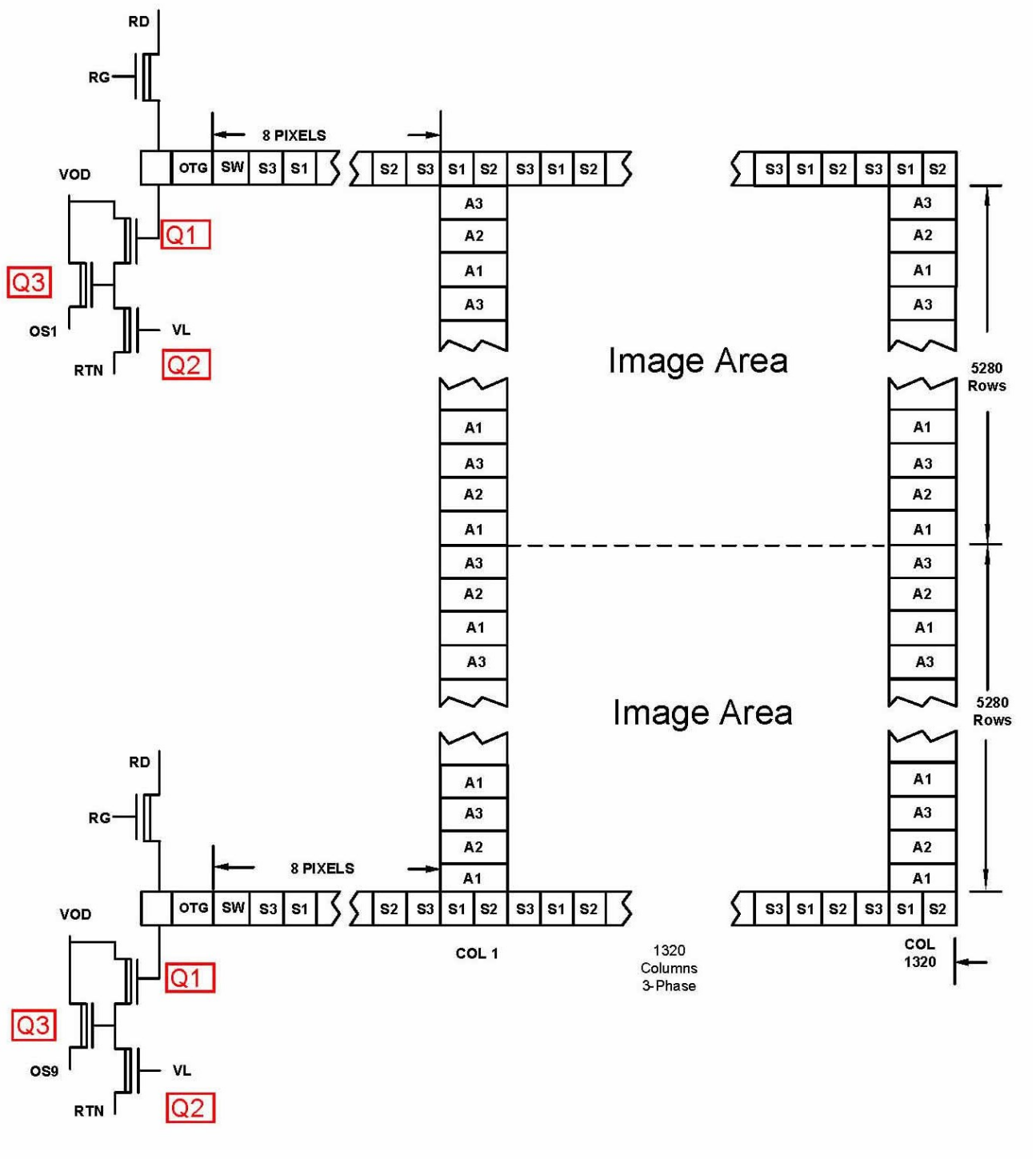
The transfer of charge into the horizontal register is the result of a vertical shift sequence. This register has 8 additional register cells between the first pixel of each line and the output amplifier. The output from these locations contains no signal and may be used as a dark level reference.

The last clocked gate in the Horizontal registers is twice as large as the others and can be used to horizontally bin charge. This gate requires its own clock, which may be tied to ϕH_2 for normal full resolution readout. The reset FET in the horizontal readout, clocked appropriately with ϕR, allows binning of adjacent pixels.

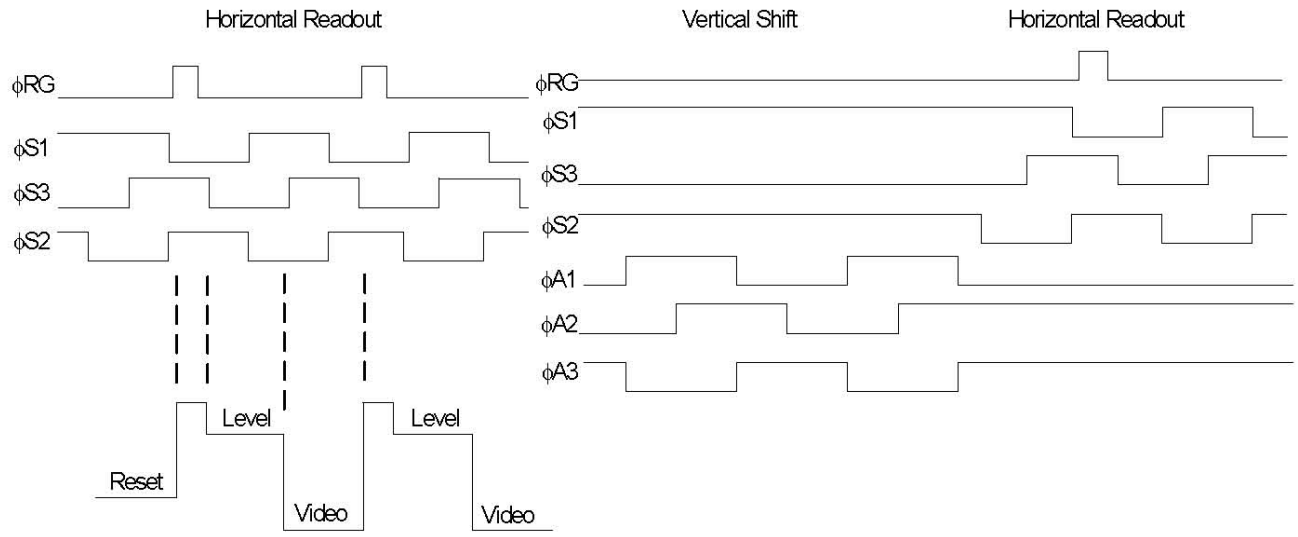
Output Amplifier: The CCD1600 has one output amplifier at the end of each Horizontal register. These are dual FET floating diffusion amplifiers with a reset MOSFET tied to the input gate.

Charge packets are clocked to a pre-charged capacitor whose potential changes linearly in response to the number of electrons delivered. When this potential is applied to the input gate of an NMOS amplifier, a signal at the output V_{out} pin is produced. The capacitor is then reset via the reset MOSFET with ϕRG to a pre-charge level prior to the arrival of the next charge packet except when horizontally binning. The output amplifier drain is tied to VDD. The source is connected to an external load resistor to ground and constitutes the video output from the device.

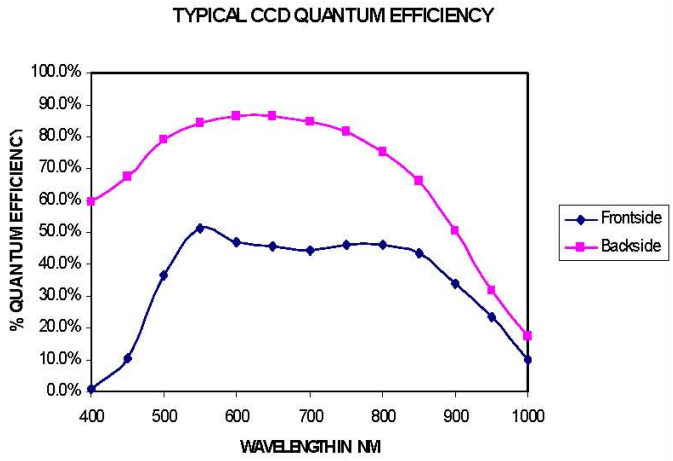
CCD1600A Schematic



Timing Diagram



Typical CCD Quantum Efficiency



Definition of Terms

Charge-Coupled Device A charge-coupled device is a monolithic silicon structure in which discrete packets of electron charge are transported from position to position by sequential clocking of an array of gates.

Vertical Transport Clocks ϕA_1, ϕA_2, ϕA_3 the clock signals applied to the vertical transport register.

Horizontal Transport Clocks ϕS_1, ϕS_2, ϕS_3 the clock signals applied to the horizontal transport registers.

Reset Clock ϕRG the clock applied to the reset switch of the output amplifier.

Dynamic Range The ratio of saturation output voltage to RMS noise in the dark. The peak-to-peak random noise is 4-6 times the RMS noise output.

Saturation Exposure The minimum exposure level that produces an output signal corresponding to the maximum photosite charge capacity. Exposure is equal to the product of light intensity and integration time.

Responsivity The output signal voltage per unit of exposure.

Spectral Response Range The spectral band over which the response per unit of radiant power is more than 10% of the peak response.

Photo-Response Non-Uniformity The difference of the response levels between the most and the least sensitive regions under uniform illumination (excluding blemished elements) expressed as a percentage of the average response.

Dark Signal The output signal is caused by thermally generated electrons. Dark signal is a linear function of integration time and an exponential function of chip temperature.

Pixel Picture element or sensor element, also called photo element or photosite

DC Operating Characteristics

Symbol	Parameter	Range min	Range nom	Range max	Unit	Remarks
V_{OD}	DC Supply Voltage		+25.0		V	
V_{RD}	Reset Drain Voltage		16.0		V	
V_{OTG}	Output Voltage	-2.0	1.0	2.0	V	
V_{VLD}	Output Load Voltage		+3.0		V	
V_{RTN}	Output Return Voltage		+2.0		V	
V_{SC}	Scupper Voltage		+20.0		V	
V_{SUB}	Substrate Ground		0.0		V	

Typical Clock Voltages

Symbol	Parameter	High	Low	Unit	Remarks
$V\phi_{S(1,2,3)}$	Horizontal Multiplexer Clock	+5.0	-5.0	V	Note 1
$V\phi_{SW}$	Summing Gate Clock	+5.0	-5.0	V	Note 1
$V\phi_{V(1,2,3)}$	Vertical Array Clocks	+3.0	-10.0	V	Note 1
$V\phi_{RG}$	Reset Array Clock	+5.0	-5.0	V	Note 1

Note 1: ϕH = 200pF, ϕV = 15,000pF. All clock rise and fall times should be > 10 ns.

AC Characteristics

Standard test conditions are nominal MPP clocks and DC operating Voltages, 1 MHz Horizontal Data Rate, 6µSec Vertical shift cycle.

Symbol	Parameter	Range min	Range nom	Range max	Unit	Remarks
V_{ODC}	Output DC Level		16.0		V	
Z	Suggested Load Register	1.0	5.0	20.0	kΩ	

Performance Specifications

Symbol	Parameter	Range min	Range nom	Range max	Unit	Remarks
V_{SAT}	Saturation Output Voltage Full Well Capacity Output Amp Sensitivity	70K	700 80K 7.0	100K	mV e- µV/e-	Note 1
PRNU	Photo Response Non-Uniformity Peak-to-Peak		10		$\%V_{SAT}$	
DSNU	Dark Signal Non-Uniformity Peak-to-Peak			1.0	mV	
DC	Dark Current	0.025	<1.0	2.0	nA/cm^2	Note 2
R	Responsivity		1.0		$V\mu j/cm^2$	
rms	Noise		5-20		e-	

Note 1: Maximum well capacity is achieved in Buried Channel Mode.
Note 2: Values shown are for 25°C. Dark current doubles for every 5°- 7°C.

Quantum Efficiency Enhancements

The CCD1600 CCD area arrays can be backside thinned for increased QE. The incident illumination enters through the backside of the array, and since no photons are absorbed in the polysilicon gate structures, the QE is increased. Also available are front side illuminated devices which can be coated with a fluorescent dye that absorbs UV light and fluoresces in the visible range. This provides CCD response at wavelengths less than 400nm.

Cosmetic Grading

Device grading helps to establish a ranking for the image quality that a CCD will provide. Blemishes are characterized as spurious pixels exceeding 10% of V_{SAT} with respect to neighboring elements. Blemish content is determined in the dark, at various illumination levels, and for different device temperatures.

The CCD1600 is available in various standard grades, as well as custom selected grades. Consult ANDANTA GmbH for available grading information and custom selections.

Warranty

Within twelve months of delivery to the end customer ANDANTA GmbH will repair or replace, at our option, any image sensor product if any part is found to be defective in materials or workmanship. Contact ANDANTA GmbH for assignment of warranty return number and shipping instructions to ensure prompt repair or replacement.

Certification

ANDANTA GmbH certifies that all products are carefully inspected and tested prior to shipment and will meet all of the specification requirements under which it is furnished

CCD1600 Image Sensor Pad Designation

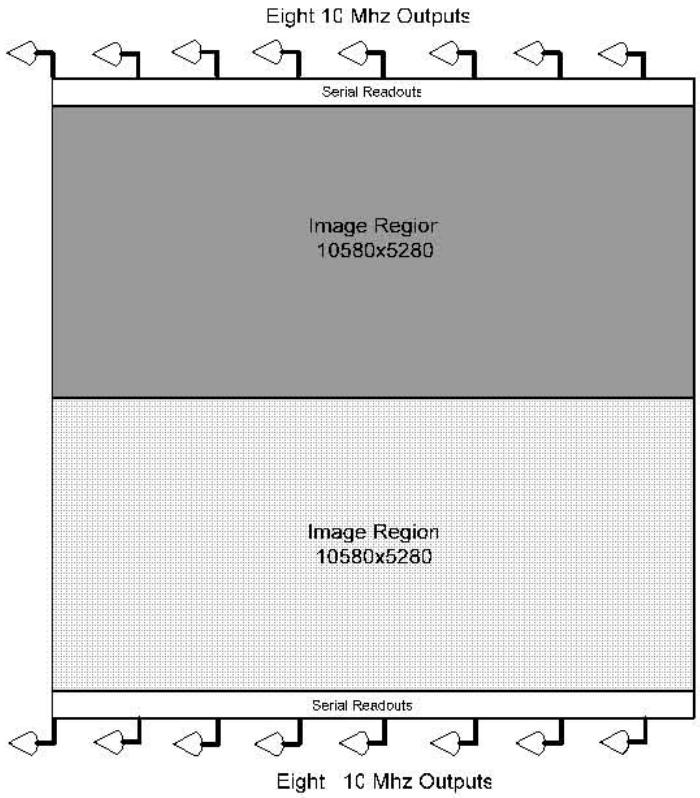
Pad#	Label
1	OS1
2	RG
3	SC
4	RD
5	SW
6	OTG
7	VLD
8	S3
9	S2
10	S1
11	RTN
12	OD
13	SUB
14	OS2
15	RG
16	SC
17	RD
18	SW
19	OTG
20	VLD
21	S3
22	S2
23	S1
24	RTN
25	OD
26	SUB
27	OS3
28	RG
29	SC
30	RD
31	SW
32	OTG
33	VLD
34	S3
35	S2
36	S1
37	RTN
38	OD
39	SUB
40	OS4
41	RG
42	SC
43	RD
44	SW
45	OTG
46	VLD
47	S3
48	S2
49	S1
50	RTN
51	OD
52	SUB
53	OS5
54	RG
55	SC
56	RD
57	SW
58	OTG
59	VLD
60	S3
61	S2
62	S1
63	RTN
64	OD

Pad#	Label
65	SUB
66	OS6
67	RG
68	SC
69	RD
70	SW
71	OTG
72	VLD
73	S3
74	S2
75	S1
76	RTN
77	OD
78	SUB
79	OS7
80	RG
81	SC
82	RD
83	SW
84	OTG
85	VLD
86	S3
87	S2
88	S1
89	RTN
90	OD
91	SUB
92	OS8
93	RG
94	SC
95	RD
96	SW
97	OTG
98	VLD
99	S3
100	S2
101	S1
102	RTN
103	OD
104	SUB
105	BB
106	SC
107	A1
108	A2
109	A3
110	SUB
111	BB
112	SC
113	A1
114	A2
115	A3
116	SUB
117	BB
118	SC
119	A1
120	A2
121	A3
122	SUB
123	BB
124	SC
125	A1
126	A2
127	A3
128	SUB

Pad#	Label
129	BB
130	SC
131	A1
132	A2
133	A3
134	SUB
135	BB
136	SC
137	A1
138	A2
139	A3
140	SUB
141	BB
142	SC
143	A1
144	A2
145	A3
146	SUB
147	BB
148	SC
149	A1
150	A2
151	A3
152	SUB
153	SUB
154	OD
155	RTN
156	S1
157	S2
158	S3
159	VLD
160	OTG
161	SW
162	RD
163	SC
164	RG
165	OS16
166	SUB
167	OD
168	RTN
169	S1
170	S2
171	S3
172	VLD
173	OTG
174	SW
175	RD
176	SC
177	RG
178	OS15
179	SUB
180	OD
181	RTN
182	S1
183	S2
184	S3
185	VLD
186	OTG
187	SW
188	RD
189	SC
190	RG
191	OS14
192	SUB

Pad#	Label
193	OD
194	RTN
195	S1
196	S2
197	S3
198	VLD
199	OTG
200	SW
201	RD
202	SC
203	RG
204	OS13
205	SUB
206	OD
207	RTN
208	S1
209	S2
210	S3
211	VLD
212	OTG
213	SW
214	RD
215	SC
216	RG
217	OS12
218	SUB
219	OD
220	RTN
221	S1
222	S2
223	S3
224	VLD
225	OTG
226	SW
227	RD
228	SC
229	RG
230	OS11
231	SUB
232	OD
233	RTN
234	S1
235	S2
236	S3
237	VLD
238	OTG
239	SW
240	RD
241	SC
242	RG
243	OS10
244	SUB
245	OD
246	RTN
247	S1
248	S2
249	S3
250	VLD
251	OTG
252	SW
253	RD
254	SC
255	RG
256	OS9

Pad#	Label
257	SUB
258	A3
259	A2
260	A1
261	SC
262	BB
263	SUB
264	A3
265	A2
266	A1
267	SC
268	BB
269	SUB
270	A3
271	A2
272	A1
273	SC
274	BB
275	SUB
276	A3
277	A2
278	A1
279	SC
280	BB
281	SUB
282	A3
283	A2
284	A1
285	SC
286	BB
287	SUB
288	A3
289	A2
290	A1
291	SC
292	BB
293	SUB
294	A3
295	A2
296	A1
297	SC
298	BB
299	SUB
300	A3
301	A2
302	A1
303	SC
304	BB



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