

CCD2900A CCD Image Sensor 4032 x 4096 Element Image Area

General Description

The CCD2900A is a 4032 x 4096 image element solid state Charge Coupled Device CCD sensor. This CCD is intended for use in high-resolution scientific, space based, industrial, and commercial electro-optical systems. The CCD2900A is organized in two halves each containing an array of 4032 horizontal by 2048 vertical photosites. The CCD2900A may be operated in either buried-channel or MPP mode. The pixel spacing is 15 μ m x 15 μ m. For dark reference, each readout line is preceded by 4 extended pixels. The dual stage output architecture allows higher frame rate operation through four readout sections. The CCD2900A is offered as a backside illuminated version for increased sensitivity and UV response in the same package configuration.

Features

- 4032 x 4096 CCD Image Array
- 15 μ m x 15 μ m Pixel
- 60.48mm x 61.44mm Image Area
- Near 100% Fill Factor
- Readout Noise Less Than 5 Electrons at 150KHz
- 4 Dual Stage 40MHz Outputs
- Three-Phase Buried Channel NMOS Image area
- Multi-pinned Phase (MPP)
- Three-Phase Buried Channel Readout Registers
- Selectable Video Output Channels

Functional Description

The following functional elements are illustrated in the block diagram:

Image Sensing Elements: Incident photons pass through a transparent polycrystalline silicon gate structure creating electron hole pairs. During integration, the collected photoelectrons are related directly to the amount of charge accumulated at each pixel. There is a linear relationship between the incident illumination intensity and the integration time.

The photosite structure is made up of a series of closely spaced MOS capacitors elements. These photosites sense light, then shift the light vertically via potential wells created by the vertical array clocks.

Vertical Charge Transfer: The charge may be shifted in one of three methods, split frame transfer to output 1,2,3 and 4, single frame transfer to outputs 1 or 2, or single frame transfer to outputs 3 or 4. At the end of an integration period the A1, A2, and A3 clocks are used to transfer charge vertically through the CCD array to the horizontal readout registers. Vertical columns are separated by a channel stop region to prevent charge migration.

The imaging area is divided into an Upper and a Lower half. Each 4032 x 2048 section may be clocked independently or together. Horizontal serial registers along the top and bottom permit simultaneous readout of both halves. The CCD2900A may be clocked such that the full array is readout by the upper or lower serial registers.

Serial, Charge Transfer: S1, S2 and S3 are polysilicon gates used to transfer charge horizontally to the output amplifiers. The horizontal serial register is twice the size of the photosite to allow for vertical binning. For both frame transfer configurations, the charge may be read out through the amplifiers at the bottom or top of the image area.

The transfer of charge into the horizontal register is the result of a vertical shift sequence. This register has 12 additional register cells between the first pixel of each line and the output amplifier. The output from these locations contains no signal and may be used as a dark level reference.

The last clocked gate in the Horizontal registers is twice as large as the others and can be used to horizontally bin charge. This gate requires its own clock, which may be tied to the next ordered serial clock for normal full resolution readout.

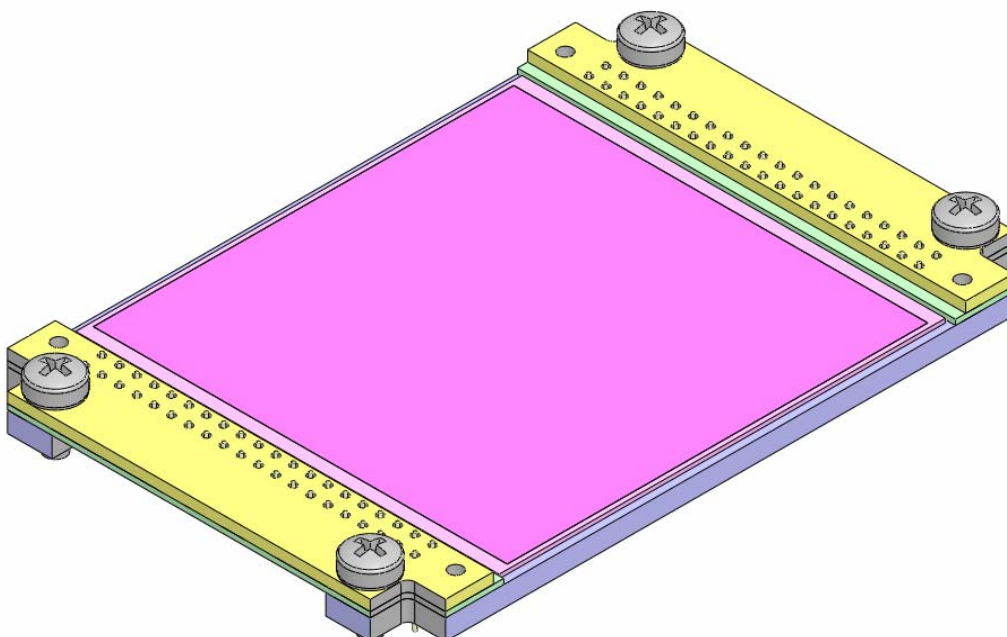
The reset FET in the horizontal readout, clocked appropriately with RG, allows binning of adjacent pixels.

Output Amplifier: The CCD2900A has four dual stage source followers that have proven low noise performance at the end of each Horizontal register.

The output capacitor is reset via the reset MOSFET with ϕ_{RG} to a pre-charge level prior to the arrival of the next charge packet except when horizontally binning.

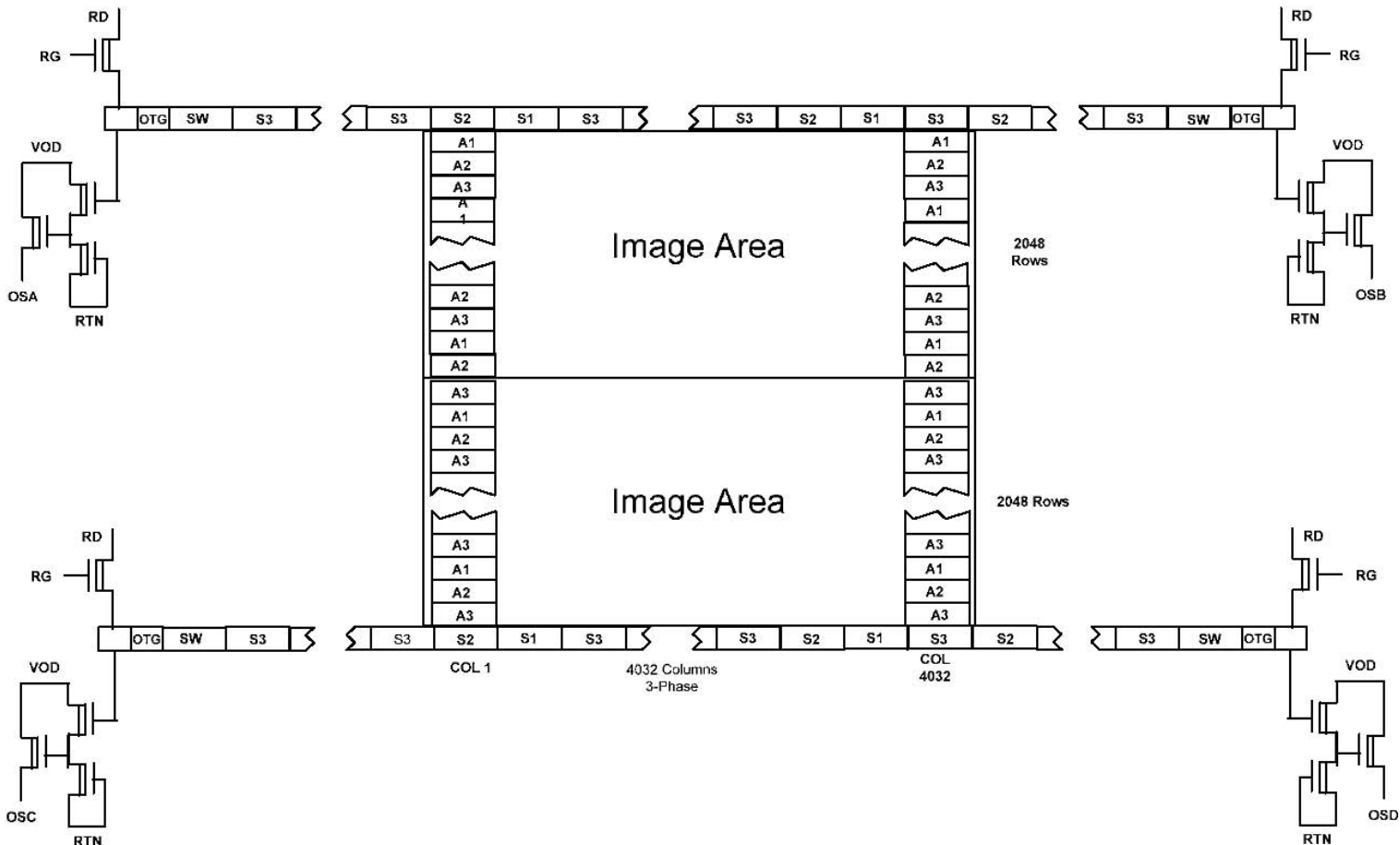
The output amplifier drains are tied to OD. The source is connected to an external load resistor to ground and constitutes the video output from the device.

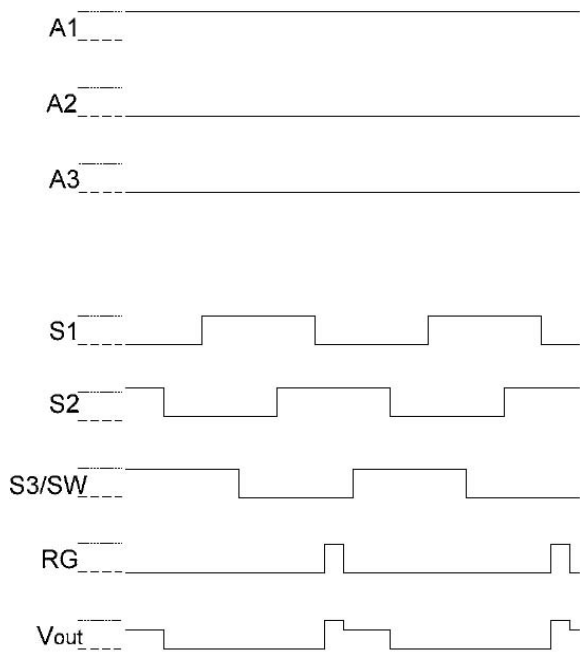
Charge packets are clocked to a pre-charged capacitor whose potential changes linearly in response to the number of electrons delivered. When this potential is applied to the input gate of an NMOS amplifier, a signal at the output V_{out} pin is produced.



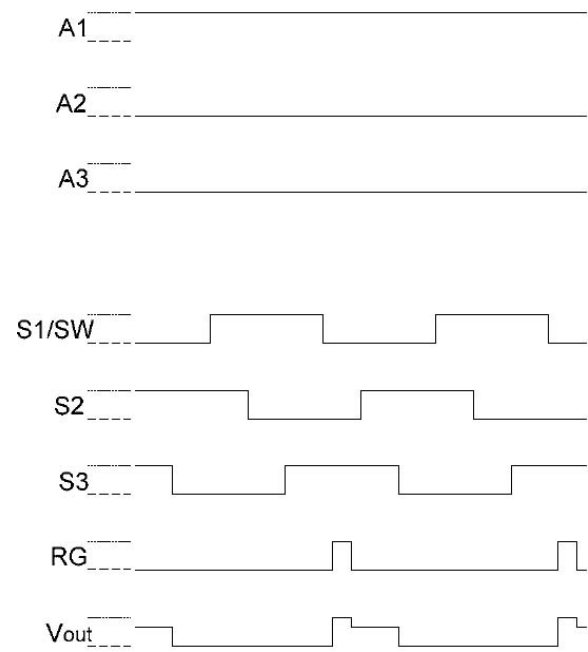
CCD2900A Pin Connections

C1		C1		C2		C2	
Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	NC	21	NC	1	NC	21	NC
2	NC	22	SCP	2	NC	22	SCP
3	OS2	23	NC	3	OS3	23	NC
4	OD	24	NC	4	OD	24	NC
5	RD	25	A2UL	5	RD	25	A2LR
6	GND	26	A3UL	6	GND	26	A3LR
7	OTG	27	A1UL	7	OTG	27	A1LR
8	SWUR	28	GND	8	SWLL	28	GND
9	NC	29	S1UL	9	NC	29	S1LR
10	RGUR	30	S2UL	10	RGLL	30	S2LR
11	S2UR	31	S3U	11	S2LL	31	S3L
12	S1UR	32	RGUL	12	S1LL	32	RGLR
13	A1UR	33	OTG	13	A1LL	33	OTG
14	GND	34	SWUL	14	GND	34	SWLR
15	A2UR	35	RD	15	A2LL	35	RD
16	A3UR	36	GND	16	A3LL	36	GND
17	GND	37	OS1	17	GND	37	OS4
18	NC	38	OD	18	NC	38	OD
19	NC	39	NC	19	NC	39	NC
20	NC	40	NC	20	NC	40	NC

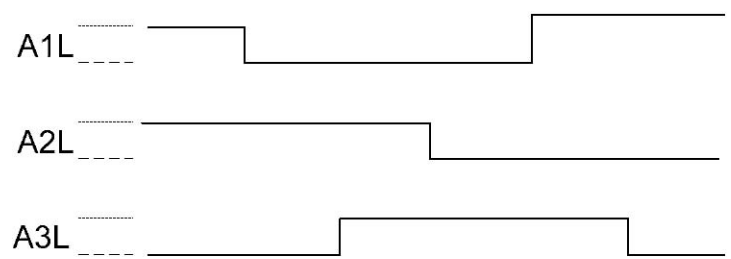




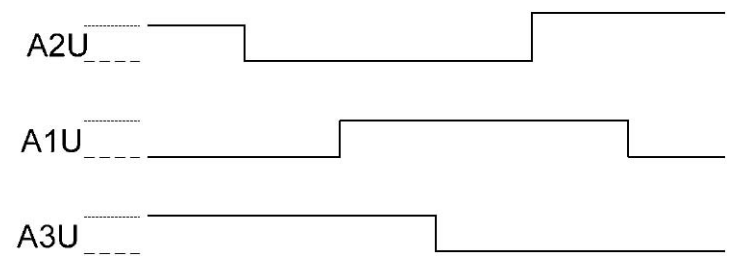
Serial readout Left 1-2-3



Serial readout Right 3-2-1



Split Frame Clock Down 1-2-3



Split Frame Clock Up 2-1-3

DC Operating Characteristics

SYMBOL	PARAMETER	RANGE			UNIT	REMARKS
		MIN	NOM	MAX		
OD	DC Supply Voltage	15.0	24.0	30.0	V	
RD	Reset Drain Voltage	10.0	15.0	20.0	V	
OTG	Output Transfer Gate Voltage	-5.0	-1.0	5.0	V	
Vss	Substrate Ground	0.0			V	

Typical Clock Voltages

SYMBOL	PARAMETER	HIGH	LOW	UNIT	REMARKS
S1,S2,S3	Horizontal Serial Clocks	+5.0	-5.0	V	Typical clock range
SW	Summing Gate Clock	+5.0	-5.0	V	Clock as S1 or S2 if not clocked separately
A1,A2,A3	Vertical Array Clocks	+3.0	-9.0	V	
RG	Reset Gate Array Clock	+8.0	-2.0	V	

AC Characteristics

SYMBOL	PARAMETER	RANGE			UNIT	REMARKS
		MIN	NOM	MAX		
V _{ODC}	Output DC Level		14.0		V	Typical
Z _{single}	Suggested Load Resistor Outputs A and D	3.0	10.0	20.0	kΩ	Higher resistance reduces bandwidth

Performance Specifications

SYMBOL	PARAMETER	RANGE			UNIT	REMARKS
		MIN	NOM	MAX		
V _{SAT}	Saturation Output Voltage Full Well Capacity	700			mV	
	Output amplifier sensitivity	100k			e-	
	Output amplifier sensitivity	7.0			μV/e-	
PRNU	Photo Response Non-Uniformity Peak-to-Peak	10			%V _{SAT}	
DSNU	Dark Signal Non-Uniformity Peak-to-Peak	1.0			mV	

Cosmetic Grading

Grading and screening of devices establishes a ranking for the image quality that a CCD provides. Blemishes are characterized as spurious pixels exceeding 10% of V_{SAT} with respect to neighbouring elements. Blemish content is determined in the dark, at various illumination levels, and for different device temperatures.

The CCD2900A CCD image sensor is available in various standard grades, as well as custom grades. Consult ANDANTA for information on grade selection.

Warranty

ANDANTA will repair or replace, at our option, any image sensor product within twelve months of delivery to the end customer, for any defect in materials or workmanship. Contact ANDANTA for further warranty information, a return number, and shipping instructions.

Certification

ANDANTA certifies that all products are carefully inspected and tested prior to shipment and will meet all of the specification requirements under the performance specifications summarized.