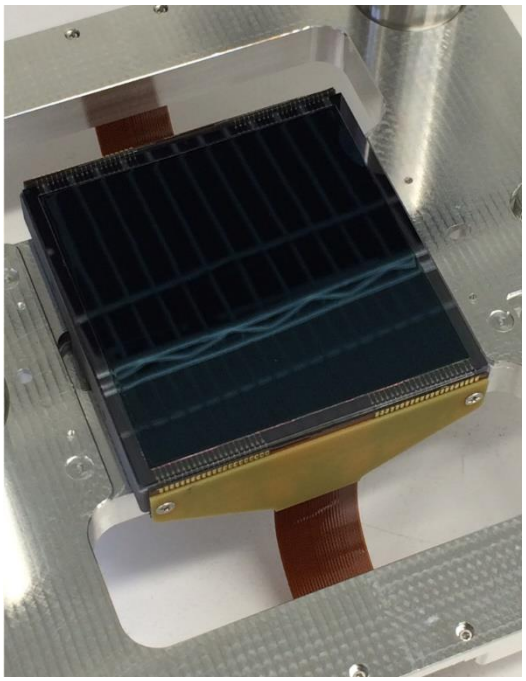
CCD 4850

4080 x 4080 Pixel CCD Image Sensor

Features

- Format: 4080 x 4080 pixels
- Pixel size: 15 µm x 15 µm
- 100% fill factor
- Readout noise: ≤3 e^- RMS at 100 kHz
- Full well capacity: >200 ke^-
- Output speed: 100 kHz - 1 MHz
- Output sensitivity: 4 µV/e^-
- 3 phase parallel and serial operation
- Coupled quadrant structure
- Any 1, 2, or 4 outputs
- Back illuminated
- Thermal time constant: ~200 s
- Thermal stability: <1 mK
- Substrate thickness: 30 or 100 µm



Description

The CCD 4850 is a 4080 X 4080 pixel buried channel Charge Coupled Device (CCD) sensor intended for use in high-resolution scientific, space-based, industrial, and commercial electro-optical systems. The CCD is organized in four coupled symmetric quadrants each containing an array of 2040 horizontal by 2040 vertical pixels. The pixel geometry is 15 µm square. The coupled symmetric design and single stage output structure allows full frame low noise operation through one, two, or four outputs.

The packaged device is offered back illuminated with a variety of anti-reflection (AR) coating options and includes an integrated temperature sensor, heater, and JFET buffer.

The CCD package is designed for ultra-high stability applications including interferometry and high resolution planet finding spectroscopy. It is made of high conductivity low thermal expansion AlSi alloy (CE6F) allowing short thermal time constants, and with the integrated sensor and heater, has the best temperature uniformity and stability ever offered in a CCD of this size. It can be mounted in one of three ways and included with an optional radiation shield, thermal isolator, and warm mounting ring. The radiation shield also doubles as a device handling jig.

Functional Description

The CCD serial (Sn) and area (An) gates are arranged such that an identical clocking pattern to each of the four quadrants results in standard four output operation.

Modification of the basic area clock pattern allows charge to be shifted up, down, or held in each of the two area clock regions independently. Modification of the basic serial clock pattern allows charge to be shifted left, right, or held in each of the four serial register regions independently. Full frame single amplifier operation is possible from any output, and full frame dual amplifier operation is possible from any pair of outputs.

The serial register pixels have approximately twice the capacity of each area pixel allowing for efficient area charge binning operation. The SG pixel is approximately twice the size of the other serial register pixels (four times the capacity of an area pixel) to allow efficient serial binning.

For optimum PRNU along the device centerlines, it is suggested that integration occurs under the A1 and A2 phases (A1 and A2 high). Charge is then shifted to the serial register in order, A1/T1 to A2/T2 to A3/S1/S2.

The dual transfer gate structure allows for stable serial readout during parallel clocking. This in turn allows for maximum pCTE with minimum overhead.

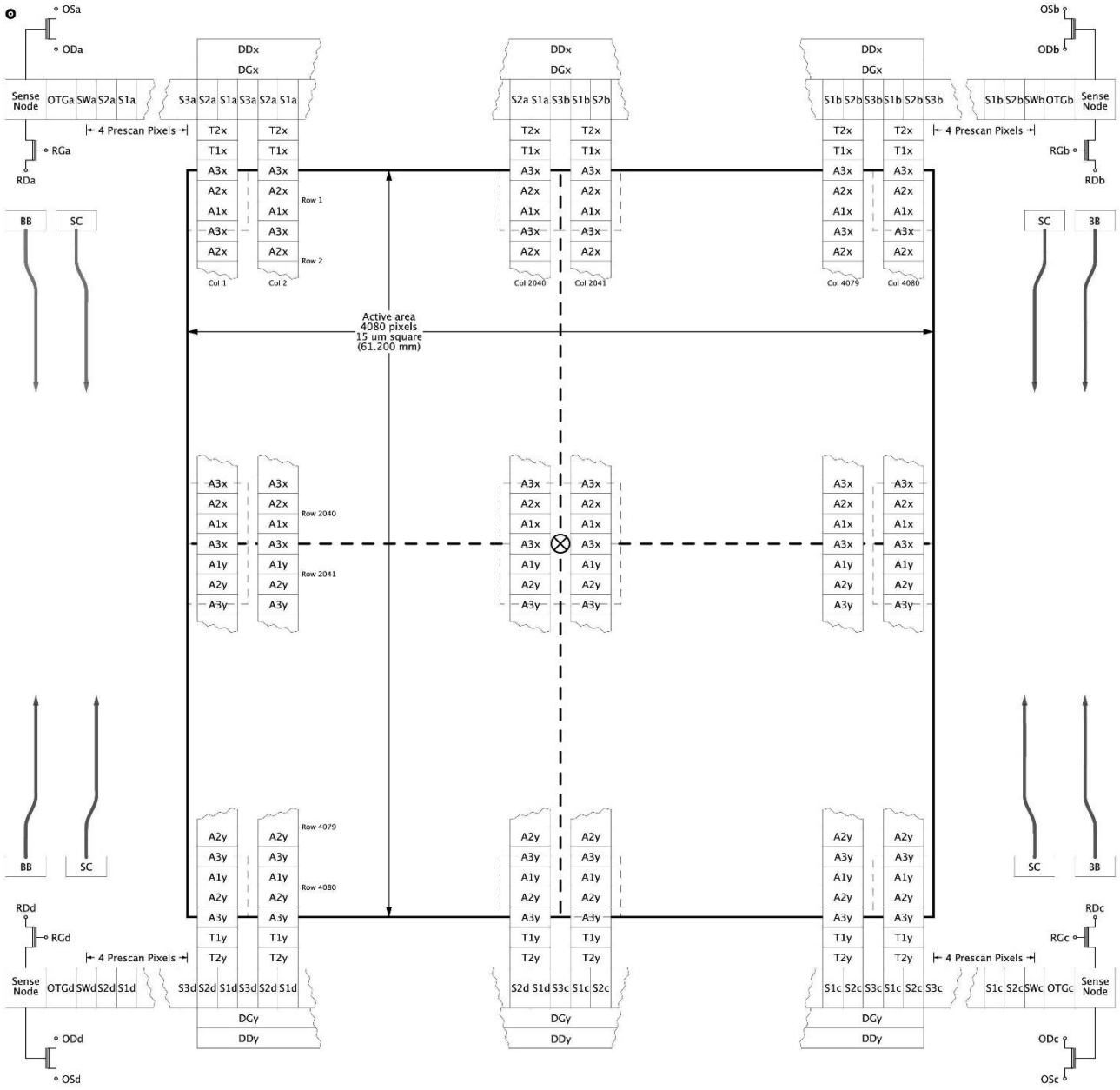
A dump drain and gate is included to allow fast array flushing and mitigate horizontal blooming from localized bright sources or defects.

Scupper regions around the image area absorb excess dark current near the edges and improve the uniformity of the DSNU structure.

Backside bias is available primarily to limit charge diffusion on 100 µm thick devices.

All four outputs are of identical design. Each is a single stage NMOS source follower that have proven low noise performance with a 1/f corner frequency below 100 kHz. Their output impedance is about 3 kOhm, but the typical package includes AC coupling and a low noise JFET source follower stage which operates at the CCD package temperature. This structure is capable, depending on output speed, of driving cabling up 1-2 m in length with minimal noise impact.

Functional Diagram



Operating point

These are nominal conditions, each device is optimized individually prior to performance characterization.

Name	Symbol	Range			Unit	Remarks
		Min	Typ	Max		
DC CHARACTERISTICS						
Output Drain voltage	OD	15	24	30	V	Must be 5-10 V greater than RD
DC reset drain voltage	RD	10	15	20	V	Must be 5-10 V less than OD
DC output transfer gate voltage	OTG	-5	-1	5	V	
DC substrate ground voltage	SS		0			
DC scupper voltage	SC		20		V	Guard ring to absorb charge produced outside the image area
DC dump drain voltage	DD		20		V	
DC Backside bias voltage	BB		-30	0	V	Limits charge diffusion in 100 um thick Si. **Should be 0 V on 30 um thick Silicon**
Recommended output load	Z_{LOAD}	3	10	20	kΩ	Higher resistance reduces on chip power dissipation and bandwidth
CLOCK CHARACTERISTICS						
Serial (horizontal) register clock voltage	S1, S2, S3	-5		5	V	Typical
Summing well clock voltage	SW	-5		5	V	Typical
Parallel (vertical) area clock voltage	A1, A2, A3, T1, T2	-9		3	V	Typical
Reset gate clock voltage	RG	-3		10	V	Typical
Dump gate voltage	DG	1		4	V	Typical
Operating temperature	T_{CCD}	-110	-100	+40	°C	

Performance specifications

A complete test report is delivered with each supplied device. All device specifications correspond to the same operating point which is supplied with the test report.

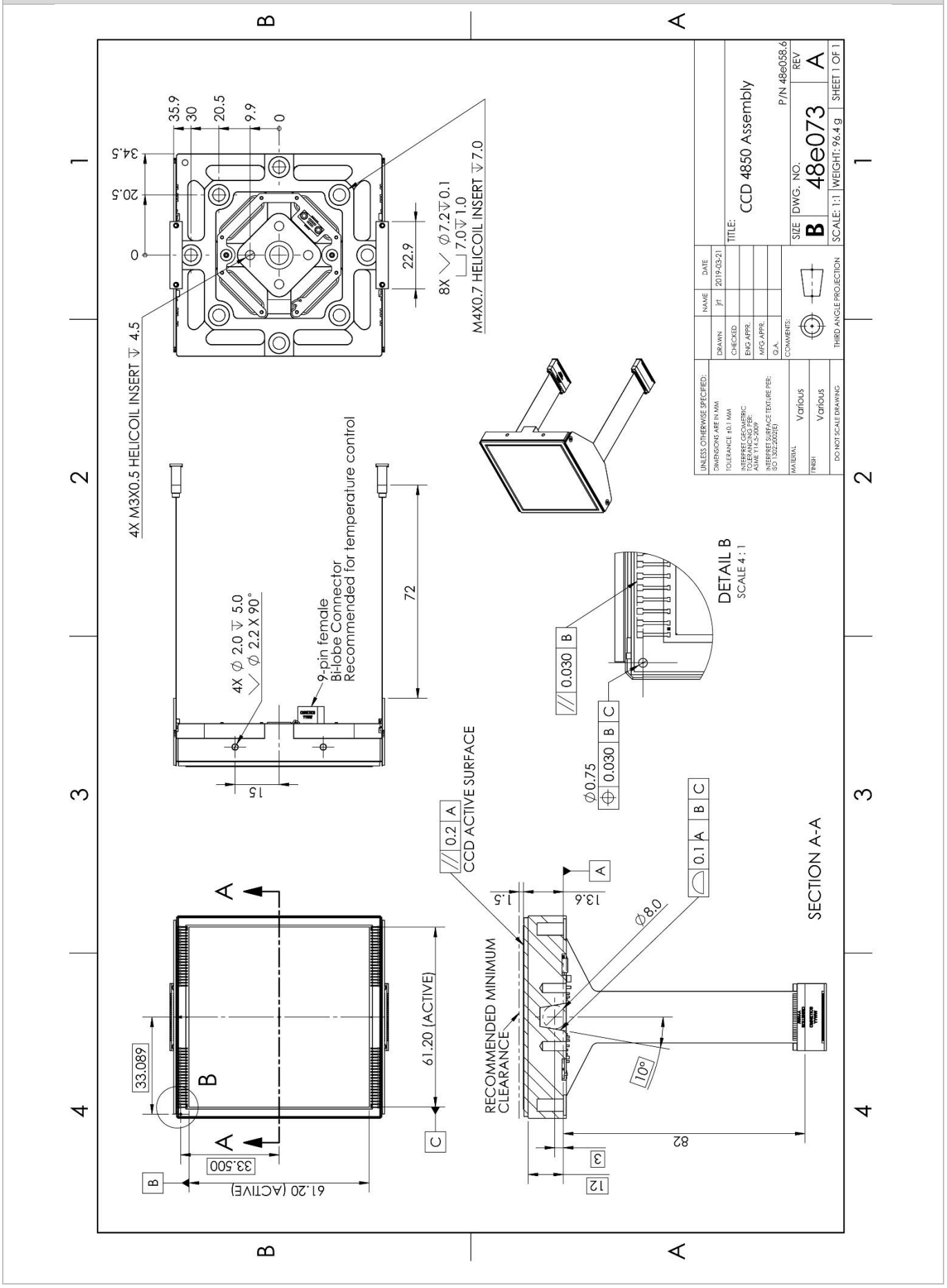
Name	Symbol	Range			Unit	Remarks
		Min	Typ	Max		
PHOTO RESPONSE						
Quantum efficiency			>90		%	At 550 nm, see figure
Photo response non-uniformity	PRNU			10	%	
Dark current			2.9	5.0	e^-/pix/h	T_{CCD} = -100 °C
DYNAMIC RESPONSE						
Image pixel capacity	FWC	200			ke^-	
Serial pixel capacity		200			ke^-	
Output node capacity		200			ke^-	
Readout noise	RN		3	4	e^-	
Non-linearity	RNL		2		%	Up to FWC
Amplifier sensitivity			4		uV/e^-	
DC output level	V_{OS}		16		V	
CHARGE TRANSFER						
Serial ineffiency	sCTI			1e-5		Per pixel
Parallel inefficiency	pCTI			1e-5		v

Mounting

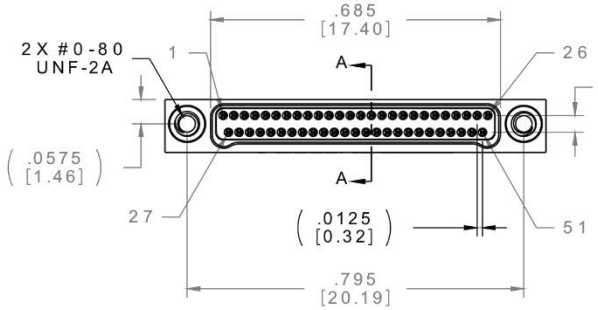
The CCD 4850 package is designed to be mounted in one of three manners according to different end uses or preferences.

- A thermal isolator can be directly attached to the CCD package for minimum thermal mass and better thermal control in high stability applications. That isolator can be trimmed on a per device basis to level and space the CCD relative to warm mounting points.
- Device specific shims and studs can be installed in a three point nearly-symmetric pattern to level the device relative to a cold mounting surface. This traditional mounting method works well for device interchangeability, but is not particularly well suited for high precision applications.
- A unique ball-in-cone or cone-in-cone mount can be used to kinematically constrain the CCD center in 3 or 5 degrees of freedom respectively. The remaining 3 or 1 degrees of freedom are then constrained with flexures attached to the edge features, while the cold thermal sink attaches in four positions near the center of each CCD quadrant. This method is ideal for ultra high precision applications like high resolution radial velocity spectrometers.

Assembly


CCD 4850 Assembly
P/N 48e058.6
SIZE B
DWG. NO. 48e073
REV A
SCALE: 1:1
WEIGHT: 96.4 g
SHEET 1 OF 1
THIRD ANGLE PROJECTION
DO NOT SCALE DRAWING
4X M3X0.5 HELICOIL INSERT ⩛ 4.5
8X ⌵ ⌀7.2⩛0.1
7.0⩛1.0
M4X0.7 HELICOIL INSERT ⩛7.0
4X ⌀ 2.0 ⩛ 5.0
⌵ ⌀ 2.2 X 90°
9-pin female
Bi-lobe Connector
Recommended for temperature control
DETAIL B
SCALE 4 : 1
CCD ACTIVE SURFACE
RECOMMENDED MINIMUM
CLEARANCE
SECTION A-A
61.20 (ACTIVE)
33.500
33.089
82
10°

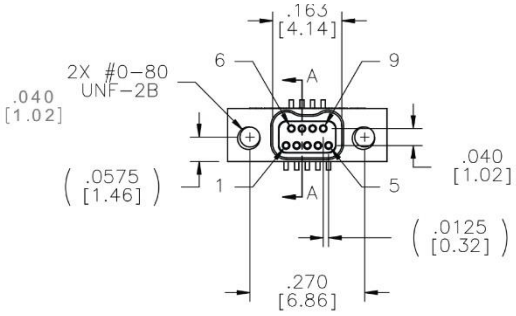
Connector Pin Configuration



Omnetics A28300-051
51-pin male Bi-Lobe connector

Pin	Signal	Pin	Signal
1	T1	27	A1L
2	T2	28	A2L
3	OD	29	A3L
4	RD	30	GND
5	OTG	31	RGL
6	GND	32	SWL
7	CCD2	33	S1L
8	CCDRTN1	34	S2L
9	GND	35	S3L
10	DG	36	HEATER+*
11	DD	37	RTD_I+*
12	SC	38	RTD I-*
13	N5V	39	GND
14	P5V	40	RTD V-*
15	BB	41	RTD V+*
16	DD	42	HEATER -*
17	DG	43	S3R
18	GND	44	S2R
19	CCD2	45	S1R
20	CCDRTN2	46	SWR
21	GND	47	RGR
22	OTG	48	GND
23	RD	49	A3R
24	OD	50	A2R
25	T2	51	A1R
26	T1		

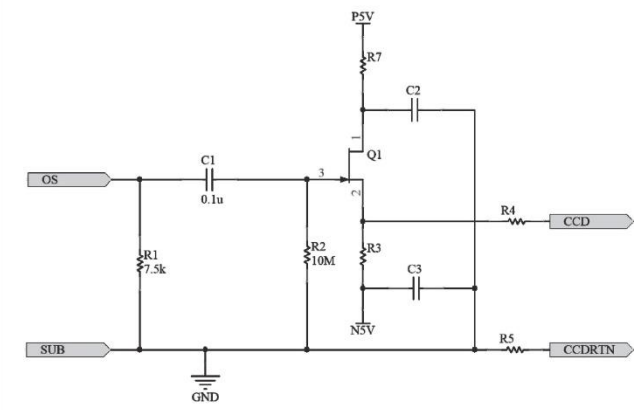
* Not recommended for use



Omnetics A29200-009
9-pin female Bi-Lobe connector

Pin	Signal
1	HEATER-
2	
3	
4	
5	HEATER+
6	RTD V+
7	RTD V-
8	RTD I-
9	RTD I+

Heater: 100 ohm, 6.25 W, 25 V max.
RTD: 1 kOhm, Pt

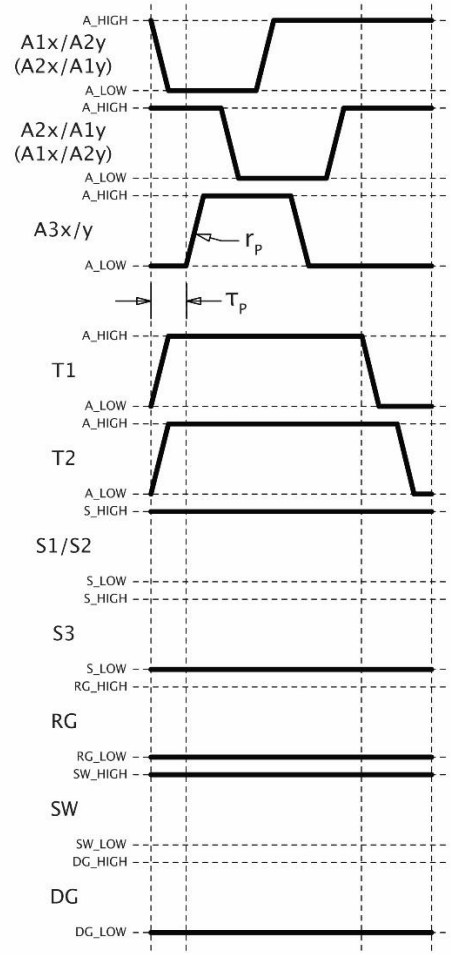


CCDn pin is connected to the CCD output source (OS) pin with buffered AC coupling.

Routines

Area shift routine

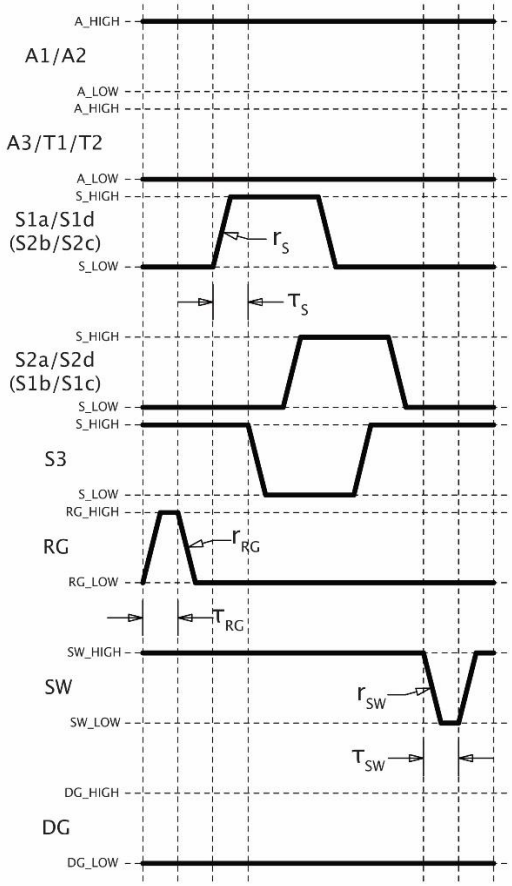
Shift parallel rows toward x (y) serial register



τ_P – Area (parallel) phase time time, 90 us
r_P – Area clock slew rate, 0.1 V/us

Read pixel routine

Shift serial pixels toward a/d (b/c) output and read.



τ_S – Serial phase time time, 120 ns
r_S – Serial clock slew rate, 200 V/us
τ_{RG} – Output node reset time, 240 ns
r_{RG} – Reset gate slew rate, 400 V/us
τ_{SW} – Summing well time, 100 ns
r_{SW} – Summing well slew rate, 200 V/us

Timing

A fast flush pixel routine is based on the read pixel routine but clocks SW the same as S3 and holds RG high during serial clocking.

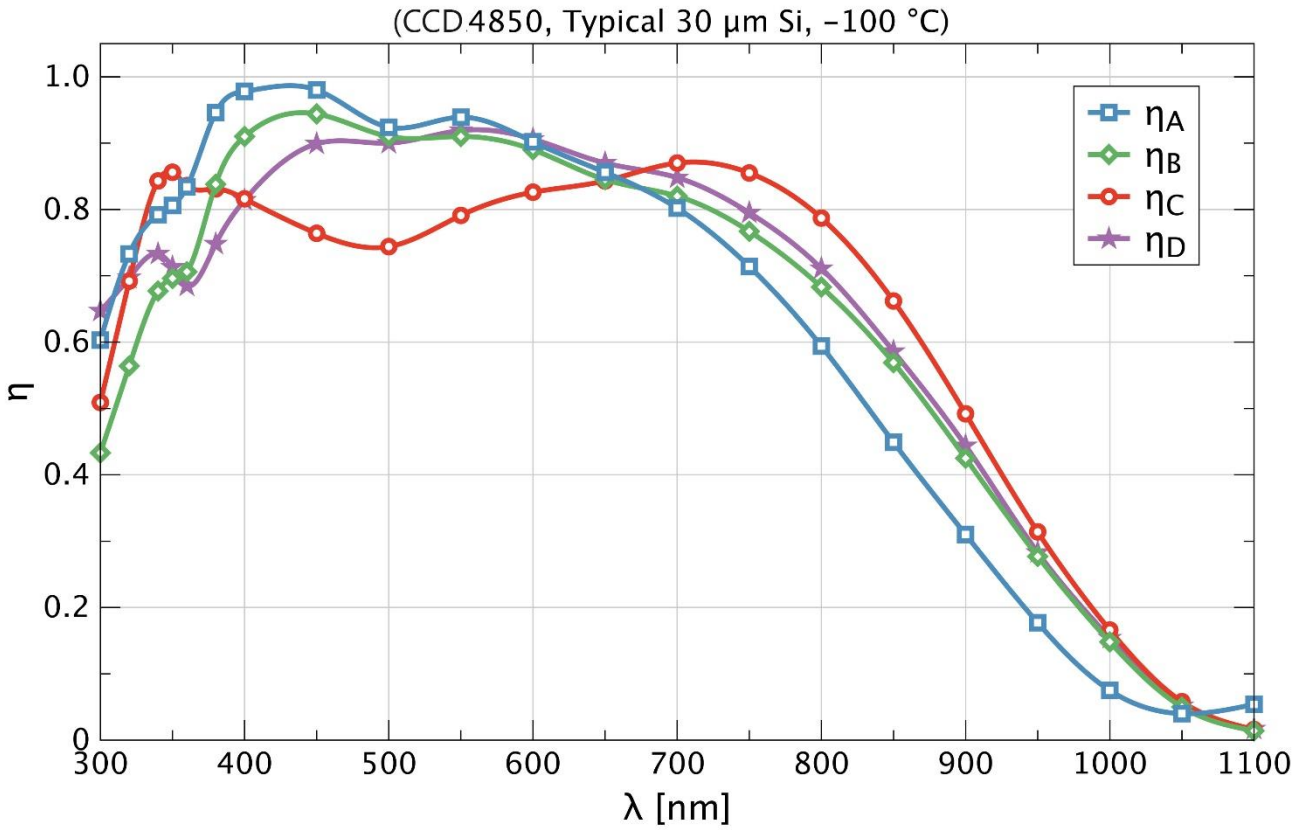
A variant of the read pixel or fast flush pixel routines is usually implemented as the integration delay loop. During integration DG is typically held high.

ANDANTA recommends flushing the serial register during integration and prior to frame readout.

For high stability applications where precision temperature control (< 1 mK) is required, it is possible to shuffle charge between the A1 and A2 phases during integration by adding them to the delay loop. This makes the mean power dissipation constant.

Quantum Efficiency

The CCD 4850 can be fabricated on either 30 µm or 100 µm thick silicon. The latter has a higher red quantum efficiency (QE). The sensor can be coated with user specified anti-reflection (AR) coatings. Typically the thinner CCD is supplied with a broadband optimized coating while the thicker is supplied with a red optimized AR coating.

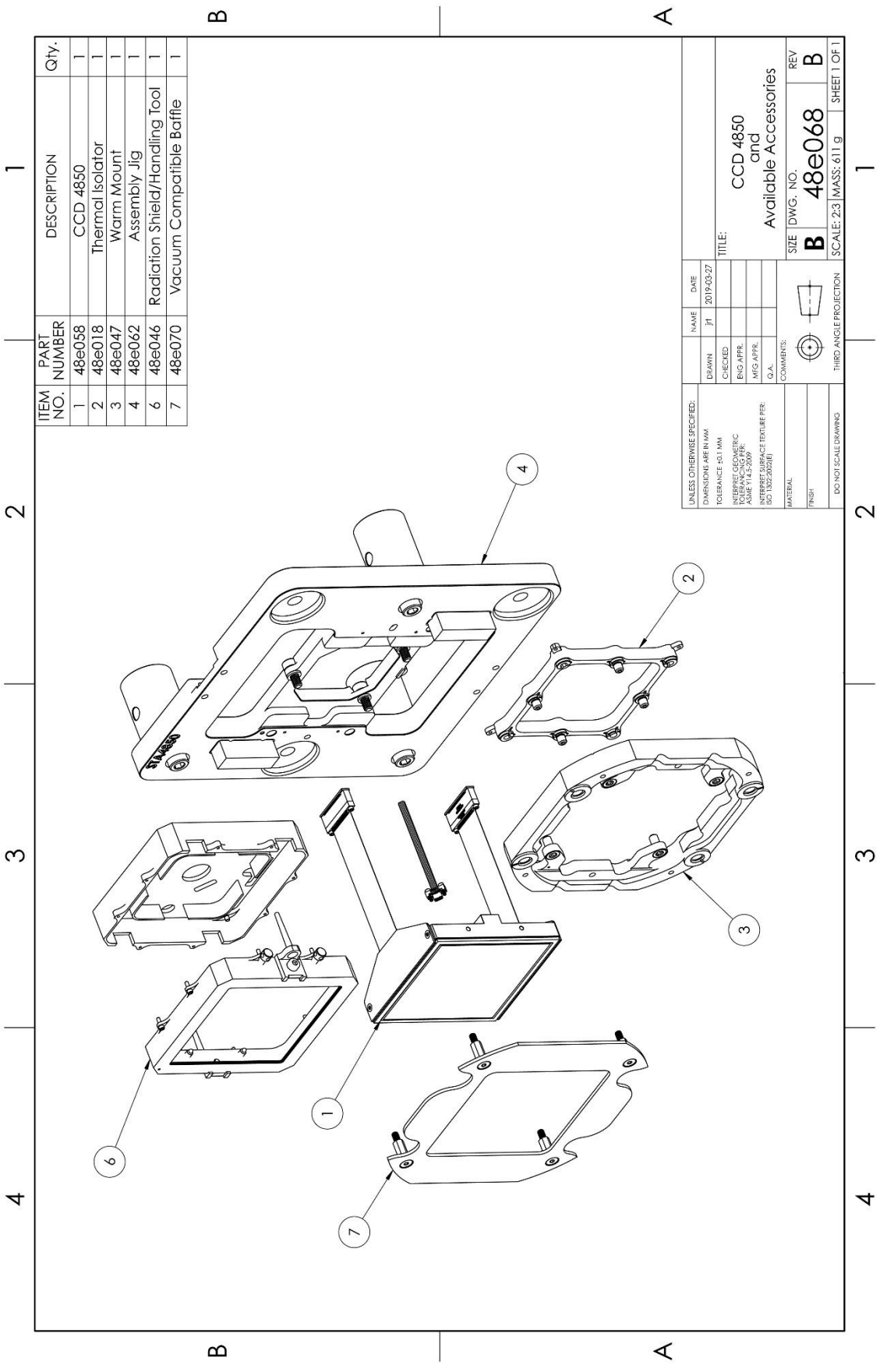


Accessories

The CCD 4850 can be supplied as a bare or packaged CCD, with various accessories, or as a complete cryogenically cooled camera system with a fitting controller. Solid models for all items are available to customers upon request.

- 48e016 Upper radiation shield and handling jig
- 48e018 Thermal isolator assembly
- 48e046 Radiation shield assembly
- 48e047 Rectangular warm mount
- 48e062 Assembly tool

Accessories



Cosmetic Grading

CCD 4850 CCDs are graded according to cosmetic defects, but custom grades are available upon request.

Specification	Grade	Range Typ	Range Max	Remarks
Column Defects	A	0	5	
	B	<5	10	An image column with >20 contiguous hot or dark pixels.
	C	<10	15	
	ENG	>15		
Hot pixels	A	<300	500	
	B	<500	800	A pixel with dark current generation of 5 e^-/pixel/s at –100 degC.
	C	<1000	1500	
	ENG	>1500		
Dark pixels	A	<200	400	
	B	<700	800	A pixel with photo-response at 532 nm of <50% of the local mean.
	C	<800	1000	
	ENG	>1000		
Trap	A	<5	10	
	B	<10	15	A pixel that temporarily holds more than 200 e– of charge.
	C	<15	20	
	ENG	>20		

Warranty

ANDANTA GmbH will repair or replace, at our option, any image sensor product within twelve months of delivery to the end customer, for any defect in materials or workmanship. Contact us for further warranty information, a return number, and shipping instructions.

Certification

ANDANTA GmbH certifies that all products are carefully inspected and tested prior to shipment and will meet all of the specification requirements under the performance specifications summarized.

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